

156 Homework Solutions #3
 Problem 4.15

Solution

The saturation current of the solar cell is calculated from:

$$I_s = qA \left[\frac{D_n n_{p0}}{w_p} + \frac{D_p p_{n0}}{L_p} \right]$$

with

$$D_n = \mu_n V_t = 1000 \times 0.0258 = 25.8 \text{ cm}^2/\text{V}\cdot\text{s}$$

$$D_p = \mu_p V_t = 300 \times 0.0258 = 7.75 \text{ cm}^2/\text{V}\cdot\text{s}$$

$$n_{p0} = n_i^2 / N_a = 10^{20} / 10^{18} = 10^2 \text{ cm}^{-3}$$

$$p_{n0} = n_i^2 / N_d = 10^{20} / 10^{16} = 10^4 \text{ cm}^{-3}$$

$$L_p = \sqrt{D_p \tau_p} = \sqrt{7.75 \times 10^{-5}} = 88 \text{ } \mu\text{m}$$

yielding $I_s = 55.5 \text{ pA}$

The maximum power is generated for:

$$\frac{dP}{dV_a} = 0 = I_s (e^{V_m/V_t} - 1) - I_{ph} + \frac{V_m}{V_t} I_s e^{V_m/V_t}$$

where the voltage, V_m , is the voltage corresponding to the maximum power point. This voltage is obtained by solving the following transcendental equation:

$$V_m = V_t \ln \frac{1 + I_{ph} / I_s}{1 + V_m / V_t}$$

Using iteration and a starting value of 0.5 V one obtains the following successive values for V_m :

$$V_m = 0.5, 0.442, 0.445 \text{ V}$$

The diode current I_m equals and the power P_m generated equals:

$$P_m = I_m \times V_m = 12.6 \text{ mW}$$

The fill factor equals:

$$\text{fill factor} = \frac{V_m I_m}{V_{oc} I_{sc}} = \frac{0.445 \times 0.0284}{0.52 \times 0.030} = 80.9 \%$$

Repeating for $I_{ph} = 300 \text{ A}$ yields:

$$\text{fill factor} = \frac{V_m I_m}{V_{oc} I_{sc}} = \frac{0.673 \times 289}{0.758 \times 300} = 85.5 \%$$

Problem 6.4 A CMOS gate requires n-type and p-type MOS capacitors with a threshold voltage of 2 and -2 Volt respectively. If the gate oxide is 50 nm what are the required substrate doping densities? Assume the gate electrode is aluminum. Repeat for a p⁺ poly-silicon gate.

Solution For nMOS (with p-type Si substrate), we have

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\epsilon_s q N_a \phi_F}}{C_{ox}}$$

where $V_{FB} = \phi_m - \chi - \frac{E_g}{2q} - \phi_F$, and $\phi_F = V_t \ln \frac{N_a}{n_i}$, if we plug

V_{FB} and ϕ_F into the equation for $V_T = 2V$, and by using iteration, we have $N_a = 7.62 \times 10^{16} \text{ cm}^{-3}$.

For pMOS (with n-type Si substrate), we have

$$V_T = V_{FB} - 2|\phi_F| - \frac{\sqrt{4\epsilon_s q N_d |\phi_F|}}{C_{ox}}$$

where $V_{FB} = \phi_m - (\chi + \frac{E_g}{2q} - |\phi_F|)$, and $|\phi_F| = V_t \ln \frac{N_d}{n_i}$, if we

plug V_{FB} and ϕ_F into the equation for $V_T = -2 \text{ V}$, and by using iteration, we have $N_d = 2.31 \times 10^{16} \text{ cm}^{-3}$.

Problem 6.6

A silicon p-MOS capacitor. ($N_d = 4 \times 10^{16} \text{ cm}^{-3}$, $t_{ox} = 40 \text{ nm}$) is biased halfway between the flatband and threshold voltage.

Calculate the applied voltage and the corresponding capacitance

Solution

For the bias halfway between the flatband and threshold voltage,

$$V_G = \frac{V_{FB} + V_T}{2} = V_{FB} - |\phi_F| - \frac{\sqrt{\epsilon_s q N_d |\phi_F|}}{C_{ox}} \quad (1),$$

$$\text{where } V_T = V_{FB} - 2|\phi_F| - \frac{\sqrt{4\epsilon_s q N_d |\phi_F|}}{C_{ox}}.$$

V_G also equals to

$$V_G = V_{FB} - \phi_s - \frac{\sqrt{2\epsilon_s q N_d \phi_s}}{C_{ox}} \quad (2).$$

We can equal (1) and (2), and get

$$|\phi_F| + \frac{\sqrt{\epsilon_s q N_d |\phi_F|}}{C_{ox}} = \phi_s + \frac{\sqrt{2\epsilon_s q N_d \phi_s}}{C_{ox}} \quad (3),$$

where $|\phi_F| = V_t \ln \frac{N_d}{n_i}$. From $N_d = 4 \times 10^{16} \text{ cm}^{-3}$ we can get

$\phi_F = 0.394 \text{ V}$, and substitute ϕ_F in equation (1) and (3) we have $V_G = -1.11 \text{ V}$ and $\phi_s = 0.28 \text{ V}$, where

$$V_{FB} = \phi_m - \left(\chi + \frac{E_g}{2q} - |\phi_F| \right).$$

From ϕ_s we can calculate $x_d = \sqrt{\frac{2\epsilon_s \phi_s}{q N_d}} = 9.6 \times 10^{-6} \text{ cm}$, and the

$$\text{total capacitance } C = \frac{1}{\frac{1}{C_{ox}} + \frac{x_d}{\epsilon_s}} = \frac{1}{\frac{t_{ox}}{\epsilon_{ox}} + \frac{x_d}{\epsilon_s}} = 48.2 \text{ nF/cm}^2.$$

Problem 7.3 A n-type MOSFET ($L = 1 \mu\text{m}$, $t_{ox} = 15 \text{ nm}$, $V_T = 1 \text{ V}$ and $\mu_n = 300 \text{ cm}^2/\text{V}\cdot\text{sec}$) must provide a current of 20 mA at a drain-source voltage of 0.5 Volt and a gate-source voltage of 5 Volt. How wide should the gate be?

Solution The MOSFET is not in saturation so that the gate width can be obtained from:

$$\begin{aligned}
 W &= \frac{I_D L}{\mu C_{ox} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}} \\
 &= \frac{0.02 \times 10^{-4}}{300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{1.5 \times 10^{-6}} \times (5 - 1 - 0.25) \times 0.5} \\
 &= 154 \text{ micron}
 \end{aligned}$$

Problem 7.10 A silicon p-substrate ($p \cong N_a = 10^{16} \text{ cm}^{-3}$) MOSFET with $t_{ox} = 0.1 \text{ } \mu\text{m}$, $\epsilon_{ox}/\epsilon_0 = 3.9$ and $V_{FB} = -0.2 \text{ V}$, has a threshold voltage which is 1 Volt smaller than desired. By what value should one change the oxide thickness, t_{ox} , to obtain the desired threshold voltage? Should one increase or decrease the oxide thickness?

Solution Similar to #7.8,

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\epsilon_s q N_a \phi_F}}{C_{ox}}$$

and one has

$$\frac{\sqrt{4\epsilon_s q N_a \phi_F}}{\epsilon_{ox}} \Delta t_{ox} = \Delta V_T = 1$$

Then $\Delta t_{ox} = 0.07 \text{ } \mu\text{m}$, and $t_{ox,2}$ should be increased to $0.17 \text{ } \mu\text{m}$ or 170nm .

Extra Problem:

Hint: An inorganic led is a PN junction and so has an band structure identical to a pn junction. An organic LED is a MIM structure so the position of the energy levels of the metal electrodes, with respect to the energy levels of the intrinsic (I) semiconductor, is important. You can draw this in flat band or at zero bias conditions, but may find flat band easier.