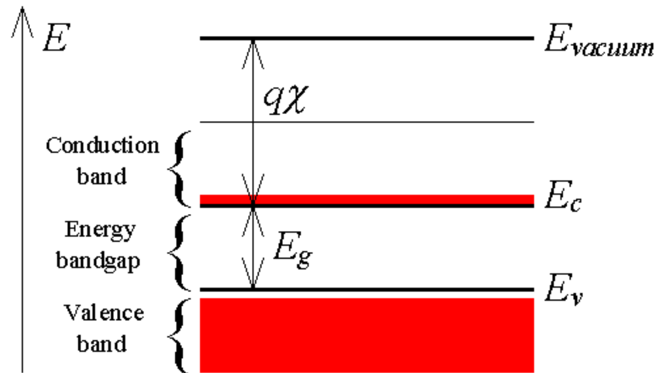
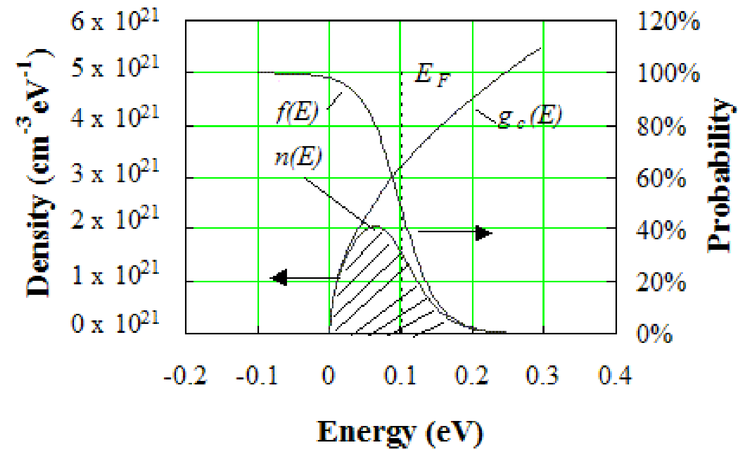
Review

Energy Bands



Carrier Density & Mobility



Carrier Transport

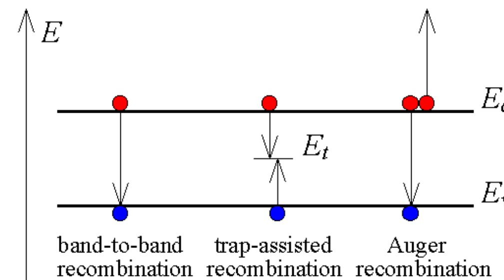
$$J_n = q n \mu_n \mathcal{E} + q D_n \frac{dn}{dx}$$

$$J_p = -q D_p \frac{dp}{dx}$$

$$\mu = \frac{q \tau_c}{m^*}$$

$$\sigma = \frac{\Delta J}{\mathcal{E}} = q(n\mu_n + p\mu_p)$$

Generation and Recombination

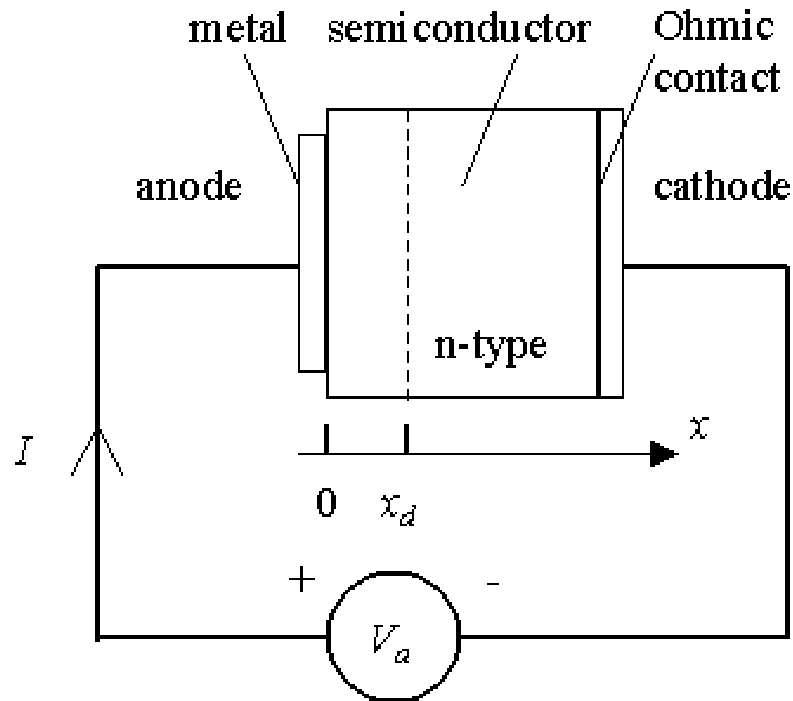


$$G_{p,light} = G_{n,light} = \alpha \frac{P_{opt}(x)}{E_{ph} A}$$

The Metal-Semiconductor Junction

To make a device, we need to connect a metal electrode to the semiconductor.

Metal-semiconductor (M-S) junctions can behave as either Schottky barriers or as Ohmic contacts, depending on the interface properties.



Ohmic contact: No potential exists between metal and semiconductor

Cathode: Electron injecting contact (low work function metal)

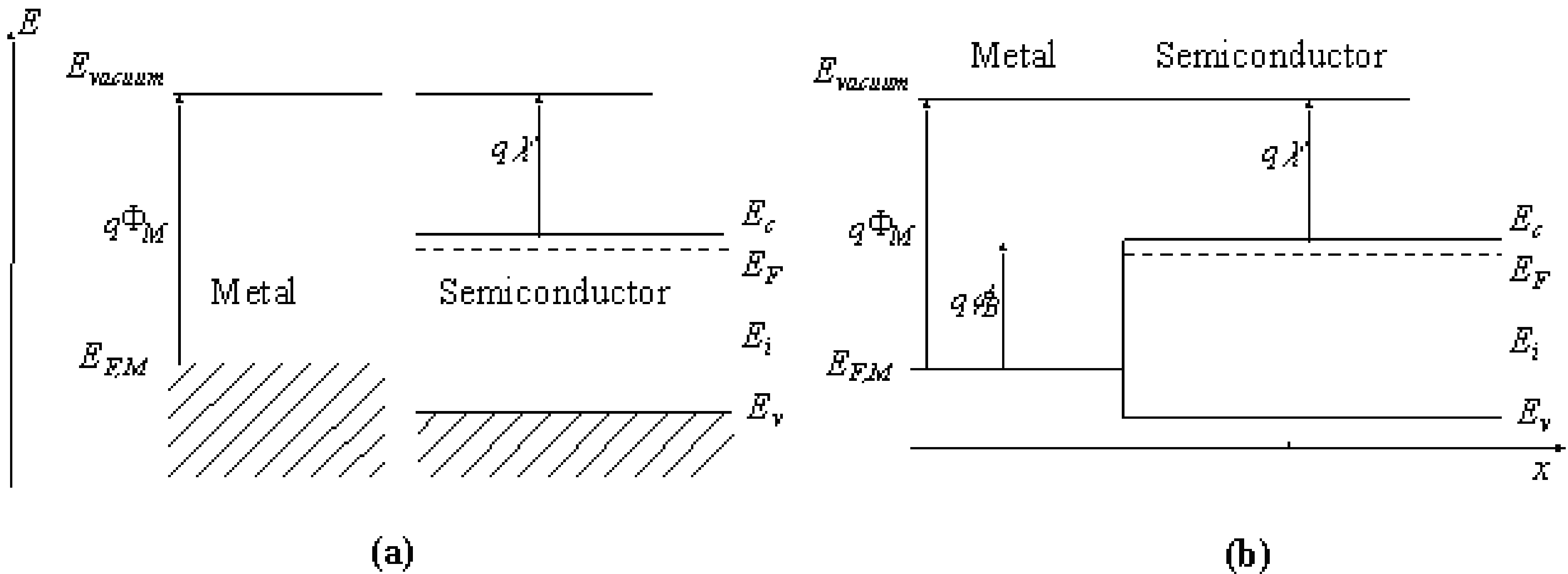
Anode: Hole injecting contact (high work function metal)

x_d: Depletion distance

Flat-band Condition

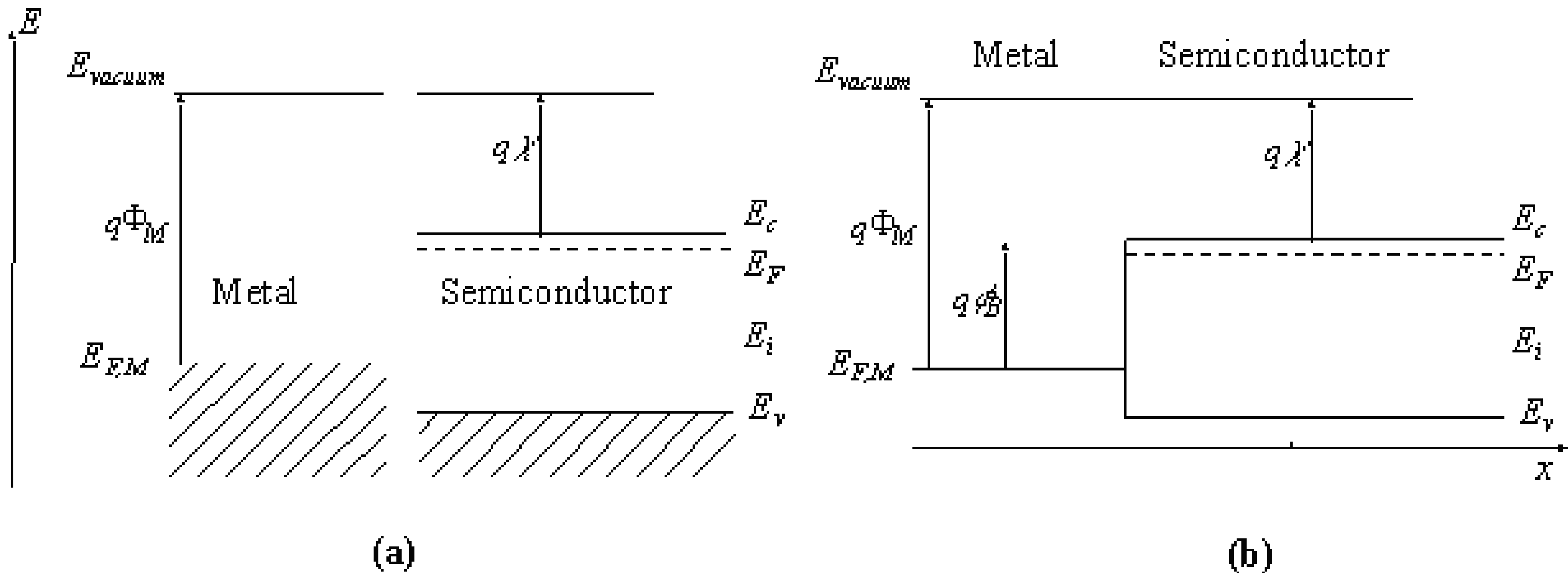
The barrier between the metal and semiconductor can be identified on energy band diagram.

As the metal and semiconductor are brought together, the Fermi energies of the metal and the semiconductor do not change right away. This yields the flatband diagram.



Energy band diagram of the metal and the semiconductor before (a) and after (b) contact

Flat-band Condition: Barrier Height



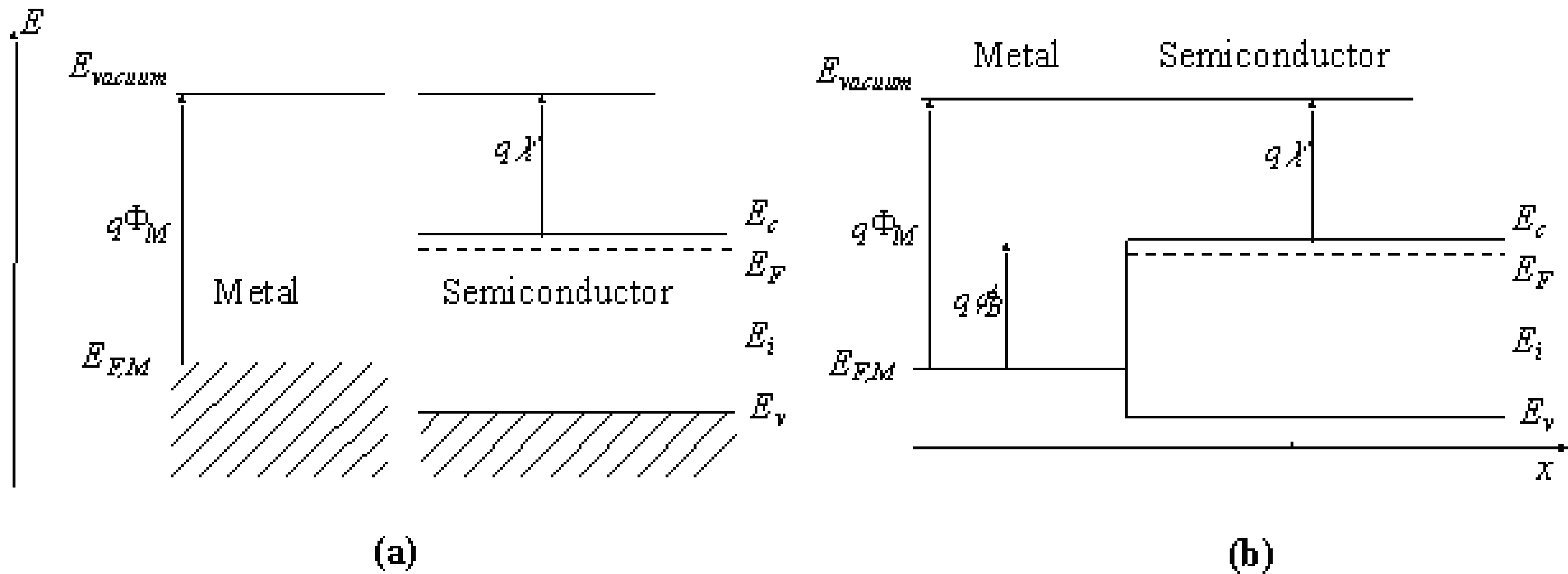
The barrier height, ϕ_B, is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carriers reside.

$$\phi_B = \Phi_M - \chi \quad \text{, for an n-type semiconductor}$$

$$\phi_B = \frac{E_g}{q} + \chi - \Phi_M \quad \text{, for a p-type semiconductor}$$

Where ϕ_M is the work function of the metal and χ is the electron affinity.

Flat-band Condition: Built-in Potential



A metal-semiconductor junction will therefore form a barrier for electrons and holes if the Fermi energy of the metal as drawn on the flatband diagram is somewhere between the conduction and valence band edge. The built-in potential, ϕ_i, is the difference between the Fermi energy of the metal and that of the semiconductor.

$$\phi_i = \Phi_M - \chi - \frac{E_c - E_{F,n}}{q} \quad , \quad \text{n-type}$$

$$\phi_i = \chi + \frac{E_c - E_{F,p}}{q} - \Phi_M \quad , \quad \text{p-type}$$

M-S Barrier Heights

	Ag	Al	Au	Cr	Ni	Pt	W
Φ_M (in vacuum)	4.3	4.25	4.8	4.5	4.5	5.3	4.6
n-Ge	0.54	0.48	0.59		0.49		0.48
p-Ge	0.5		0.3				
n-Si	0.78	0.72	0.8	0.61	0.61	0.9	0.67
p-Si	0.54	0.58	0.34	0.5	0.51		0.45
n-GaAs	0.88	0.8	0.9			0.84	0.8
p-GaAs	0.63		0.42				

Workfunction in units of eV of selected metals and their measured barrier height on germanium, silicon and gallium arsenide. These experimental barrier heights often differ from the calculated using ones.

The ideal metal-semiconductor theory assumes that both materials are infinitely pure, that there is no interaction between the two materials and no unwanted interfacial layer. Chemical reactions between the metal and the semiconductor alter the barrier height as do interface states at the surface of the semiconductor and interfacial layers.

Barrier heights reported in the literature to vary widely due to different surface cleaning procedures.

M-S Barrier Heights

Example 3.1 Consider a chrome-silicon metal-semiconductor junction with $N_d = 10^{17}$ cm^{-3}. Calculate the barrier height and the built-in potential at room temperature. Repeat for a p-type semiconductor with the same doping density.

$$\phi_B = \Phi_M - \chi = 4.5 - 4.05 = 0.45 \text{ V}$$

$$\phi_i = \Phi_M - \chi - \frac{E_c - E_{F,n}}{q} \quad , \quad \text{n-type}$$

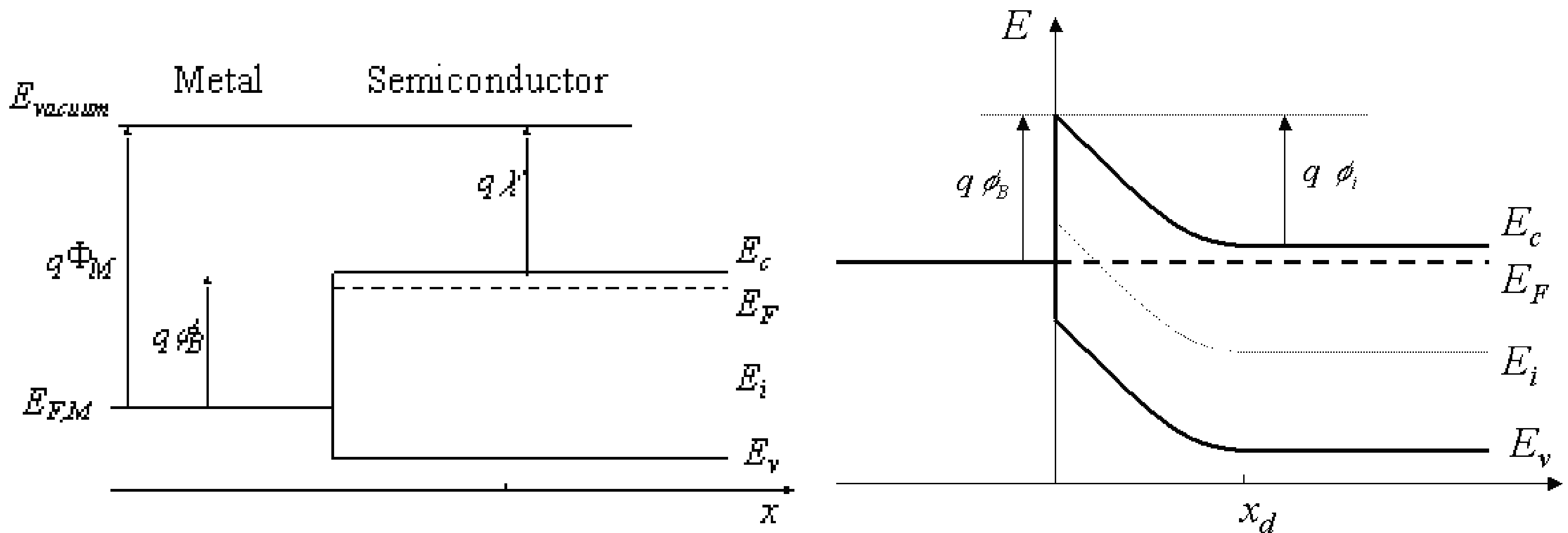
$$\phi_i = \phi_B - kT \frac{N_c}{N_d} = 0.45 - 0.0259 \ln \frac{2.82 \times 10^{19}}{10^{17}} = 0.30 \text{ V}$$

$$\phi_B = \chi + \frac{E_g}{q} - \Phi_M = 4.05 + 1.12 - 4.5 = 0.67 \text{ V}$$

$$\phi_i = \phi_B - kT \frac{N_v}{N_a} = 0.67 - 0.0259 \ln \frac{1.83 \times 10^{19}}{10^{17}} = 0.53 \text{ V}$$

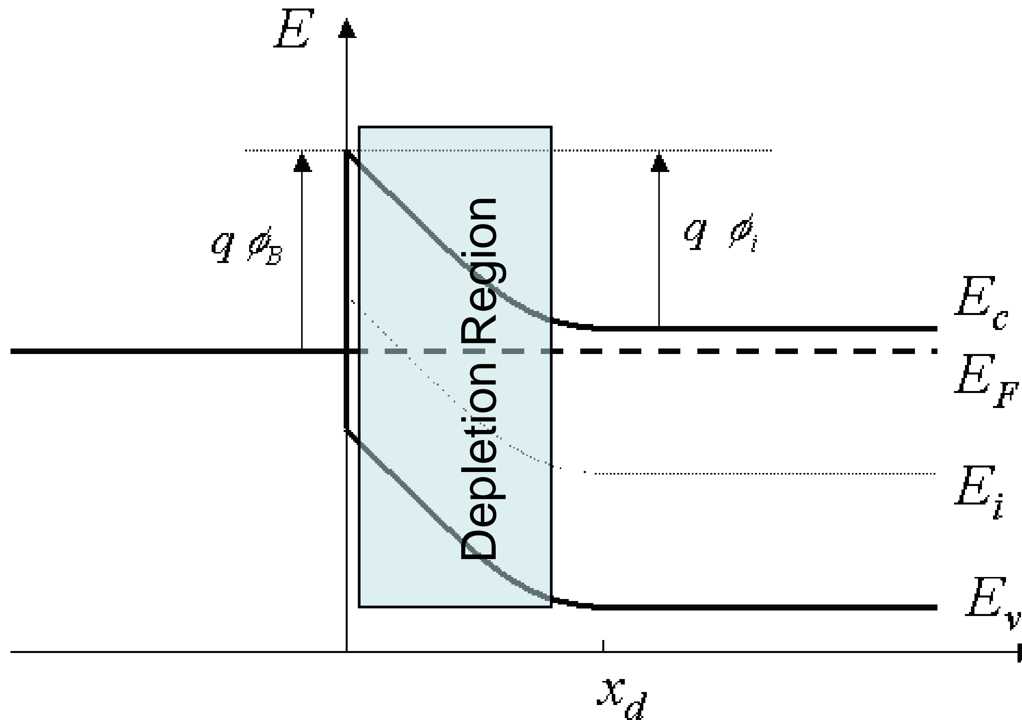
M-S Junctions: Thermal Equilibrium

The flatband diagram is not a thermal equilibrium diagram, since the Fermi energy in the metal differs from that in the semiconductor. Electrons in the n-type semiconductor can lower their energy by traversing the junction. As the electrons leave the semiconductor, a positive charge, due to the ionized donor atoms, stays behind. This charge creates a negative field and lowers the band edges of the semiconductor. Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by the ionized impurity atoms. This equilibrium is characterized by a constant Fermi energy throughout the structure.



Energy band diagram of a metal-semiconductor contact in thermal equilibrium.

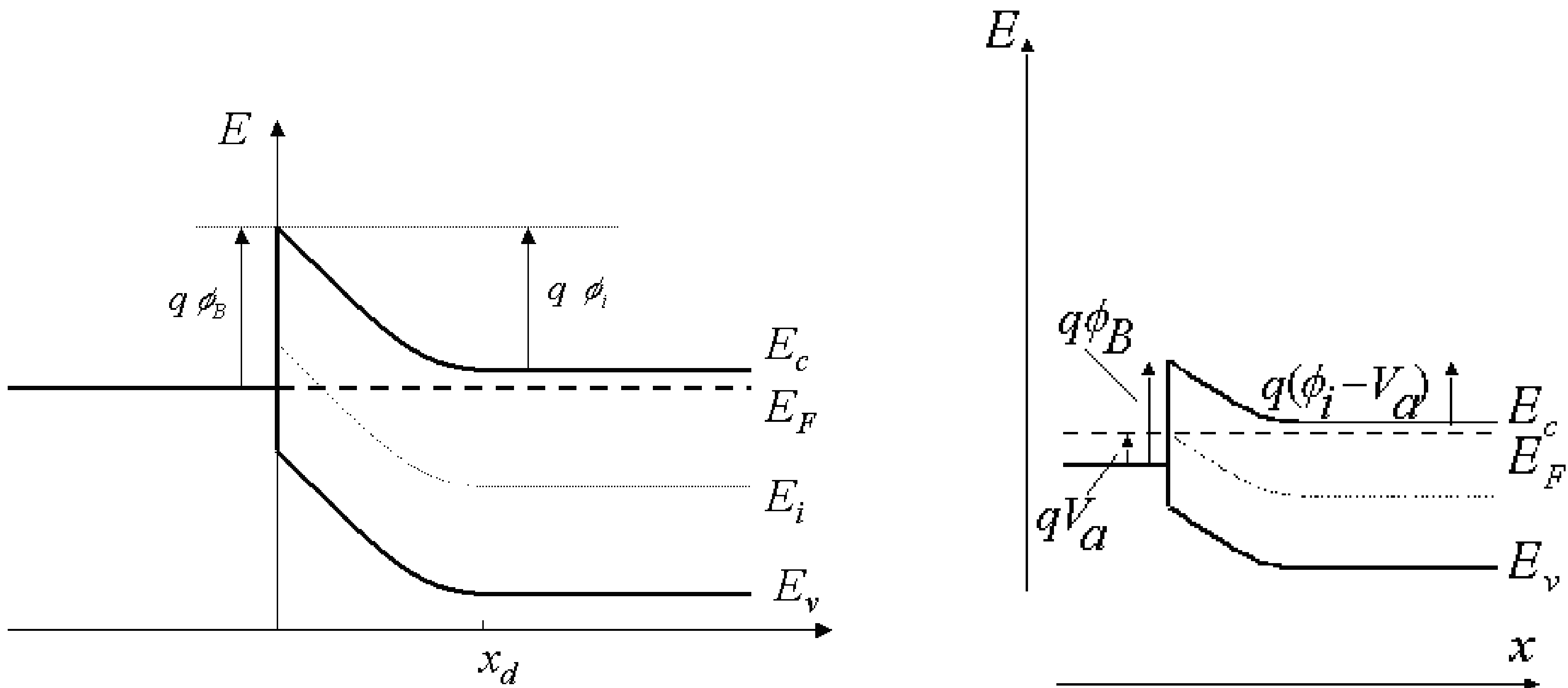
M-S Junctions: The Depletion Region



In thermal equilibrium (no external voltage applied), a region exists in the semiconductor close to the junction which is depleted of mobile carriers. This is called the **depletion region**. The potential across the semiconductor equals the built-in potential, ϕ_i.

M-S Junctions: Forward Bias

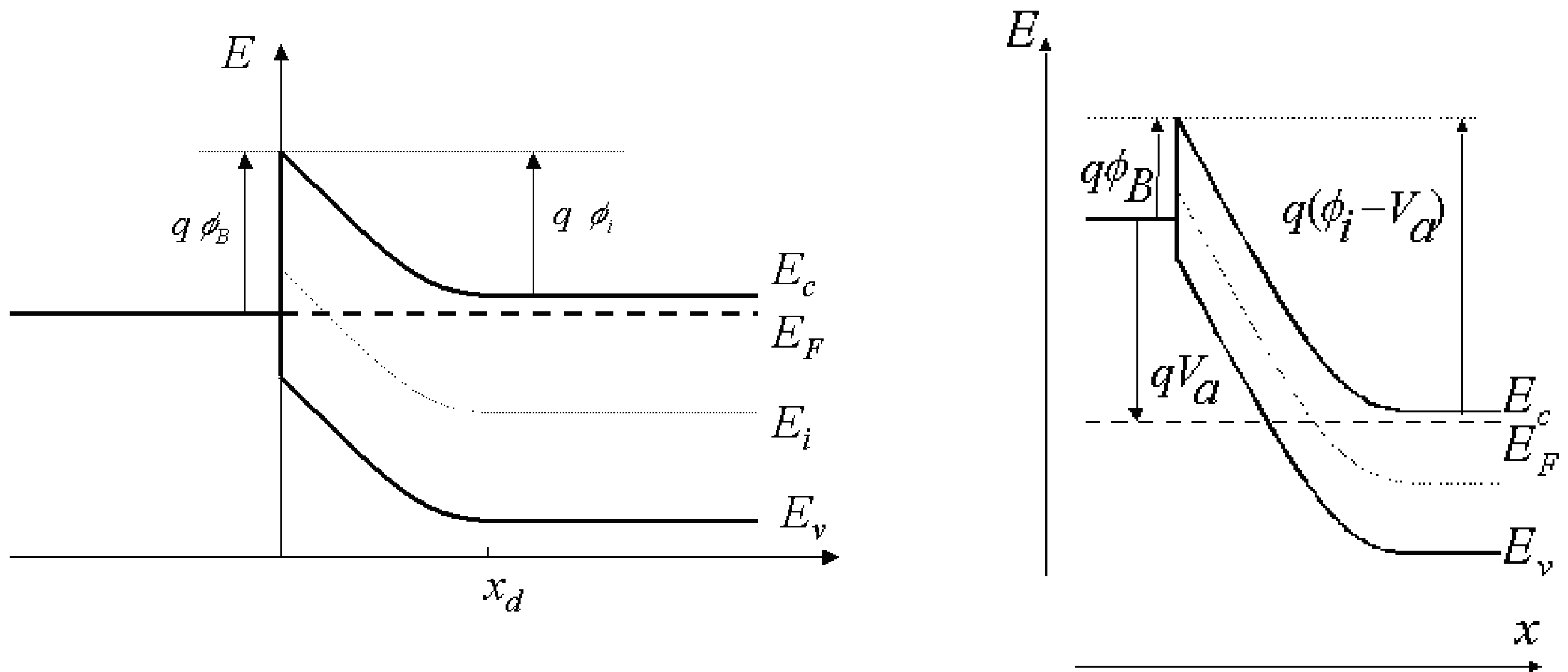
As a positive bias is applied to the metal, the Fermi energy of the metal is lowered with respect to the Fermi energy in the semiconductor. This results in a smaller potential drop across the semiconductor. The balance between diffusion and drift is disturbed and more electrons will diffuse towards the metal than the number drifting into the semiconductor. This leads to a positive current through the junction at a voltage comparable to the built-in potential.



A M-S junction under forward bias

M-S Junctions: Reverse Bias

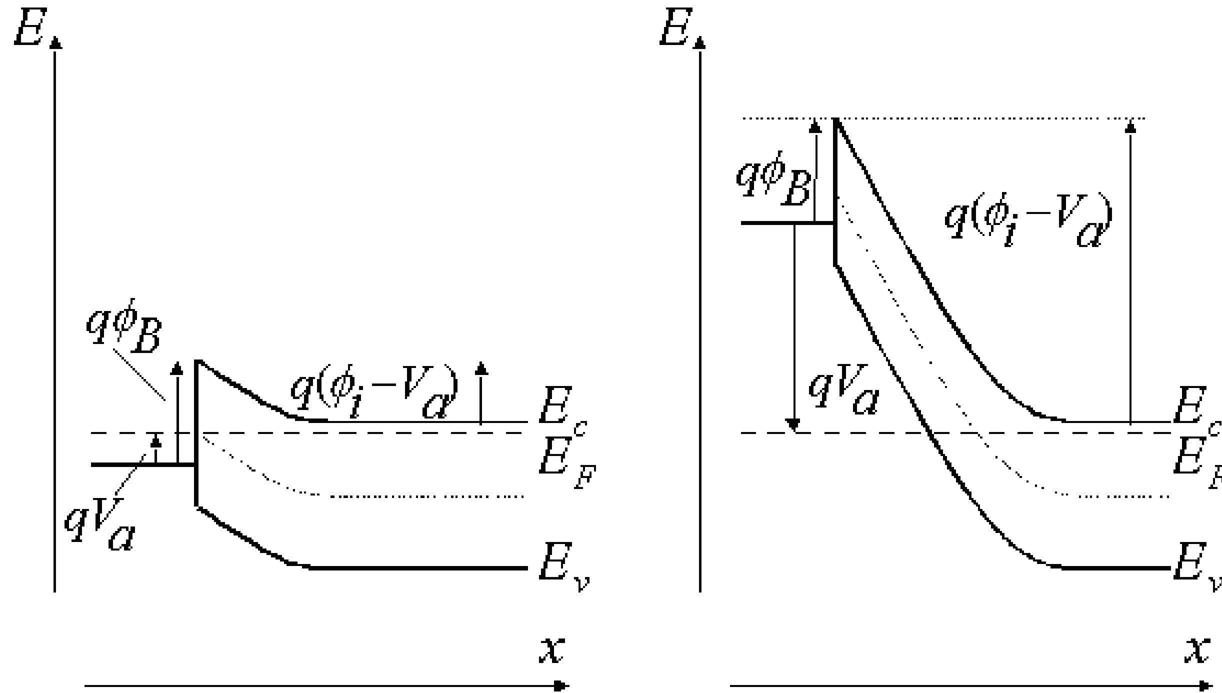
As a negative voltage is applied,the Fermi energy of the metal is raised with respect to the Fermi energy in the semiconductor. The potential across the semiconductor now increases, yielding a larger depletion region and a larger electric field at the interface. The barrier, which restricts the electrons to the metal, is unchanged so that that barrier, independent of the applied voltage, limits the flow of electrons.



A M-S junction under reverse bias

The metal-semiconductor junction with positive barrier height has a rectifying behavior. A large current exists under forward bias, while almost no current exists under reverse bias.

M-S Junctions Under Bias



The potential across the semiconductor therefore equals the built-in potential, ϕ_i, minus the applied voltage, V_a.

$$\phi(x = \infty) - \phi(x = 0) = \phi_i - V_a$$

Analysis of M-S Junction: Poisson's Equation

Electrostatic analysis of M-S junction provides info on charge and field in depletion region.

Poisson's equation (from E&M):

$$\frac{d\phi(x)}{dx} = -\mathcal{E}(x) \qquad \frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon}$$

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\varepsilon_s} = -\frac{q}{\varepsilon_s}\left(p - n + N_d^+ - N_a^-\right)$$

where the charge density, ρ, is written as a function of the electron density n, the hole density p and the donor and acceptor densities N_d and N_a. To solve the equation, we have to express the electron and hole density, n and p, as a function of the potential, φ:

$$\frac{d^2\phi}{dx^2} = \frac{2qn_i}{\varepsilon_s}\left(\sinh\frac{\phi - \phi_F}{V_t} + \sinh\frac{\phi_F}{V_t}\right) \qquad \sinh\frac{\phi_F}{V_t} = \frac{N_a^- - N_d^+}{2n_i}$$

This second-order non-linear differential cannot be solved analytically.

Analysis of M-S Junction: Full depletion approximation

We define the depletion region to be between the metal-semiconductor interface ($x = 0$) and the edge of the depletion region ($x = x_d$). To find the depletion layer width, we start with the charge density in the semiconductor and calculate the electric field and the potential across the semiconductor as a function of the depletion layer width. We then solve for the depletion layer width by requiring the potential across the semiconductor to equal the difference between the built-in potential and the applied voltage, $\phi_i - V_a$.

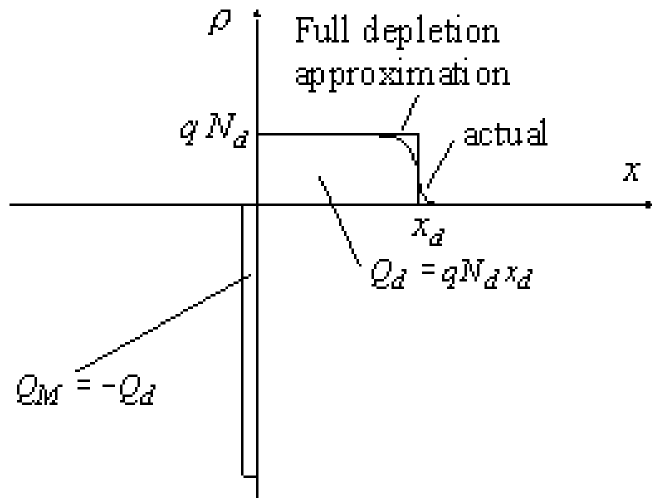
As the semiconductor is depleted of mobile carriers within the depletion region, the charge density in that region is due to the ionized donors. Outside the depletion region, the semiconductor is assumed neutral.

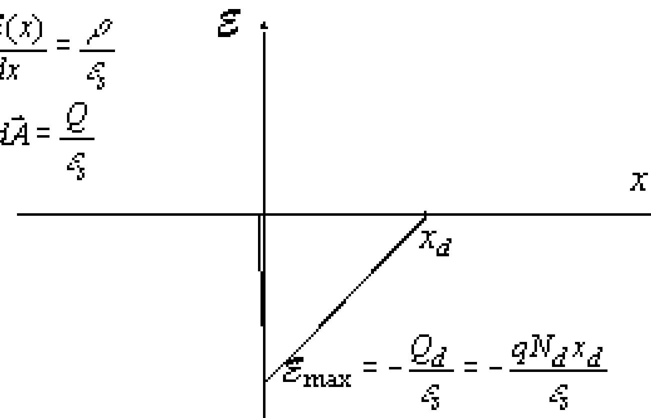
$$\rho(x) = qN_d \qquad 0 < x < x_d$$

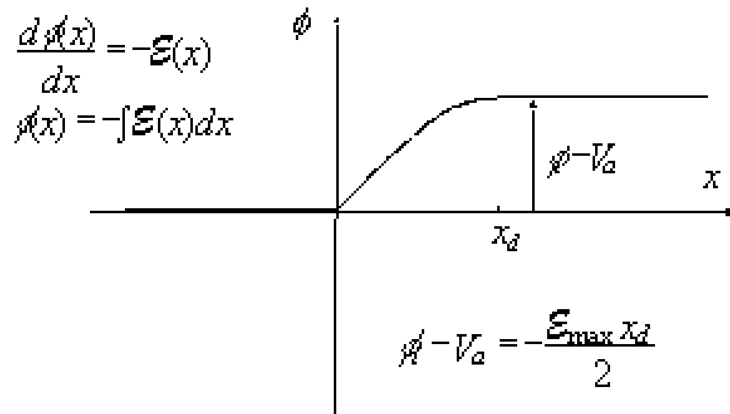
$$\rho(x) = 0 \qquad x_d < x$$

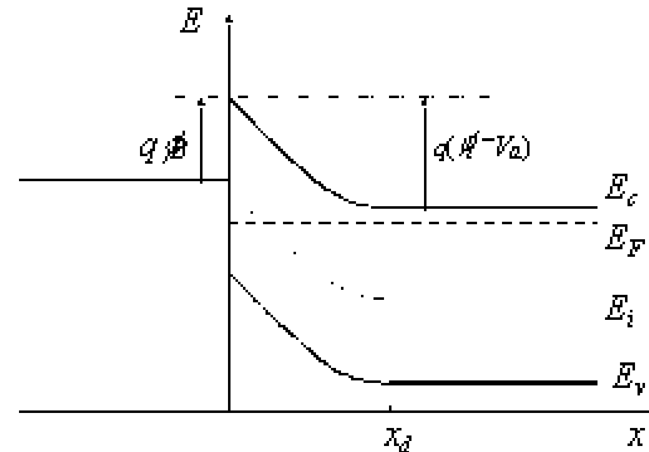
where we assumed full ionization so that the ionized donor density equals the donor density, N_d.

Analysis of M-S Junction: Full depletion approximation









(a) Charge density, (b) electric field, (c) potential and (d) energy with the full depletion analysis.

Analysis of M-S Junction: Gauss's Law for Electric Field

Gauss's Law: $$\frac{d\mathcal{E}(x)}{dx} = \frac{\rho(x)}{\varepsilon}$$

$$\rho(x) = qN_d \qquad 0 < x < x_d$$
$$\rho(x) = 0 \qquad x_d < x$$

$$\mathcal{E}(x) = -\frac{qN_d}{\varepsilon_s}(x_d - x) \qquad 0 < x < x_d$$

$$\mathcal{E}(x) = 0 \qquad x_d \leq x$$

where ε_s is the dielectric constant of the semiconductor and the electric field is assumed to be zero outside the depletion region. The largest electric field is at the interface:

$$\mathcal{E}(x = 0) = -\frac{qN_d x_d}{\varepsilon_s} = -\frac{Q_d}{\varepsilon_s}$$

where Q_d is the total charge (per unit area in the depletion layer.

Analysis of M-S Junction: Obtain x_d

Since the electric field is minus the gradient of the potential, one obtains the potential by integrating the expression for the electric field, yielding:

$$\phi(x) = 0 \qquad x \le 0$$

$$\phi(x) = \frac{qN_d}{2\varepsilon_s}[x_d^2 - (x_d - x)^2] \qquad 0 < x < x_d$$

$$\phi(x) = \frac{qN_d x_d^2}{2\varepsilon_s} \qquad x_d \le x$$

The total potential difference across the semiconductor equals the built-in potential in thermal equilibrium and is further reduced/increased by the applied voltage when a positive/negative voltage is applied to the metal as described by equation. This boundary condition provides the following relation between the semiconductor potential at the surface, the applied voltage and the depletion layer width:

$$\phi_i - V_a = -\phi(x = 0) = \frac{qN_d x_d^2}{2\varepsilon_s}$$

$$x_d = \sqrt{\frac{2\varepsilon_s(\phi_i - V_a)}{qN_d}}$$

Analysis of M-S Junction: Capacitance

The capacitance as a function of the applied voltage is the derivative of the charge with respect to the applied voltage yielding:

$$C_j = \left|\frac{dQ_d}{dV_a}\right| = \sqrt{\frac{q\,\varepsilon_s N_d}{2(\phi_i - V_a)}} = \frac{\varepsilon_s}{x_d}$$

Parallel Plate Capacitor: $C \sim \varepsilon A/d$

While the parallel plate capacitor expression seems to imply that the capacitance is constant, the metal-semiconductor junction capacitance is not constant since the depletion layer width, x_d, varies with the applied voltage.

Analysis of M-S Junction: Capacitance

Example 3.2 Consider a chrome-silicon M-S junction with $N_d = 10^{17}$ cm^{-3}. Calculate the depletion layer width, the electric field in the silicon at the M-S interface, the potential across the semiconductor and the capacitance per unit area for an applied voltage of -5 V.

$$x_d = \sqrt{\frac{2\varepsilon_s(\phi_i - V_a)}{qN_d}}$$

$$= \sqrt{\frac{2 \times 11.9 \times 8.85 \times 10^{-14} \times (0.3 + 5)}{1.6 \times 10^{-19} \times 10^{17}}} = 0.26$$

$$\mathcal{E}(x = 0) = \frac{qN_d x_d}{\varepsilon_s}$$

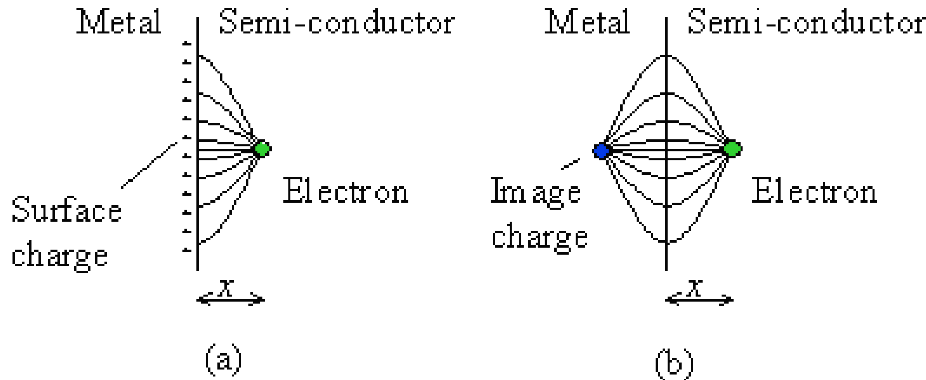
$$= \frac{1.6 \times 10^{-19} \times 10^{17} \times 2.6 \times 10^{-5}}{11.9 \times 8.85 \times 10^{-14}} = 4.0 \times 10^5 \text{ V/cm}$$

$$\phi(x = x_d) = \frac{qN_d x_d^2}{2\varepsilon_s} = \phi_i - V_a = 5.3 \text{ V}$$

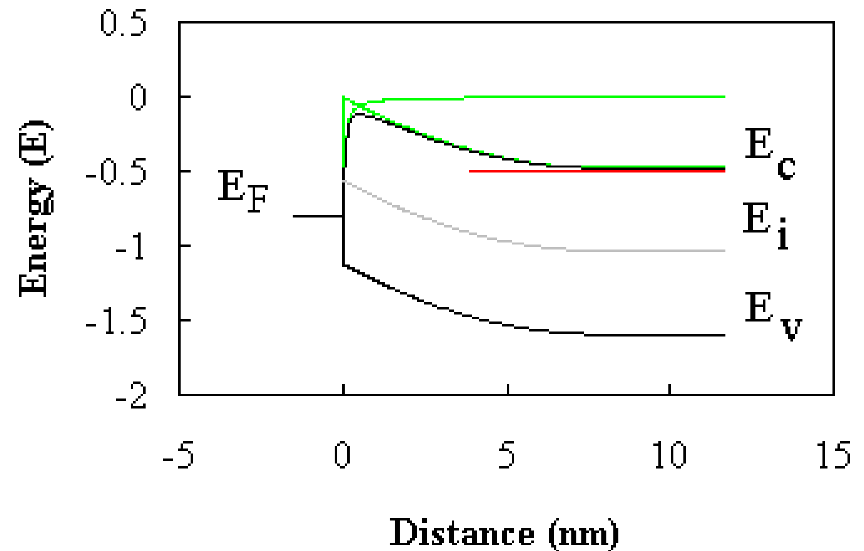
$$C_j = \frac{\varepsilon_s}{x_d} = \frac{11.9 \times 8.85 \times 10^{-14}}{2.6 \times 10^{-5}} = 40 \text{ nF/cm}^2$$

Schottky Barrier Lowering

Image charges build up in the metal electrode of a M-S junction as carriers approach the interface. The potential associated with these charges reduces the effective barrier height. This barrier reduction is small but depends on the applied voltage and leads to a voltage dependence of the reverse bias current. Note that this barrier lowering is only experienced by a carrier while approaching the interface and not be noticeable in a C-V measurement.



a) Field lines and surface charges due to an electron in close proximity to a perfect conductor and b) the field lines and image charge of an electron.

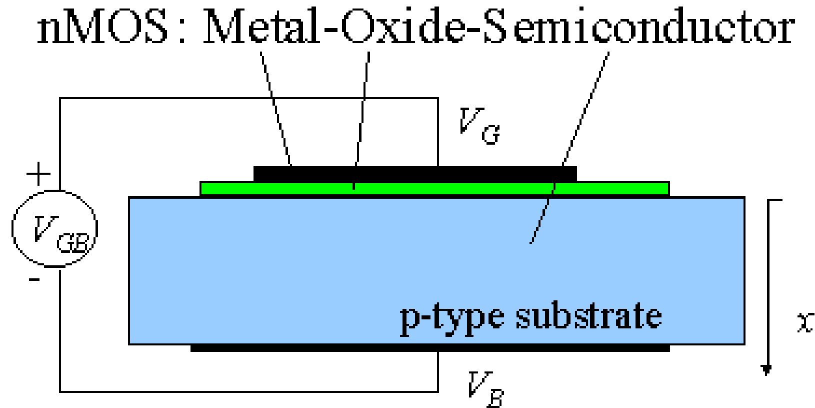


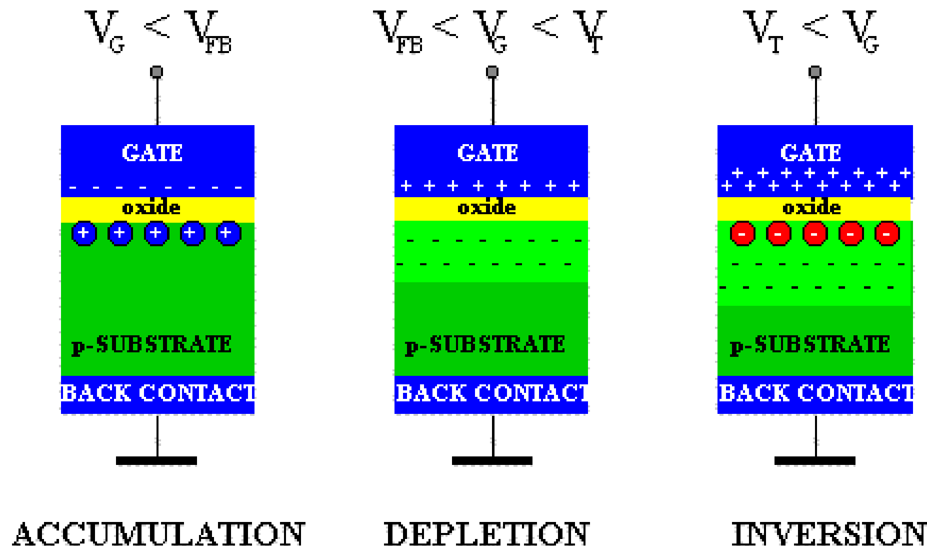
Energy band diagram of a silicon Schottky barrier with ϕ_B = 0.8 V and $N_d = 10^{19}$ cm^{-3}.

$$\Delta \phi_B = \sqrt{\frac{q \mathcal{E}_{max}}{4 \pi \varepsilon_s}}$$

MOS Capacitors

The MOS capacitor consists of a Metal-Oxide-Semiconductor structure





Three operating regions:

Accumulation: -V -- charges accumulate at oxide-semiconcutor surface

Depletion: +V -- pushes mobile holes into substrate. The semiconductor is depleted of mobile charge carriers at interface.

Inversion: ++V -- beyond VT, minority carriers are attracted to the interface forming a negative inversion layer.

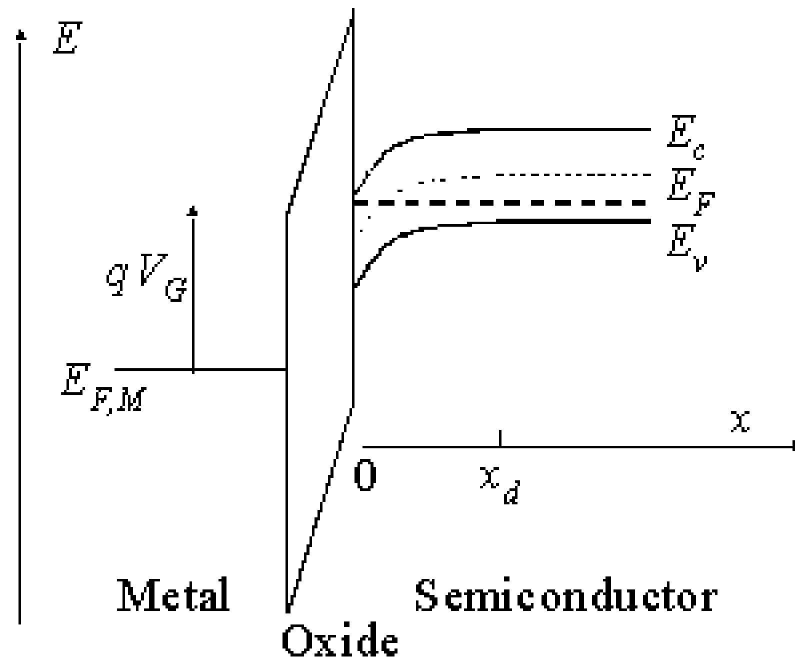
V_G = Gate Voltage

V_T = Threshold Voltage

V_{FB} = Flat Band Voltage

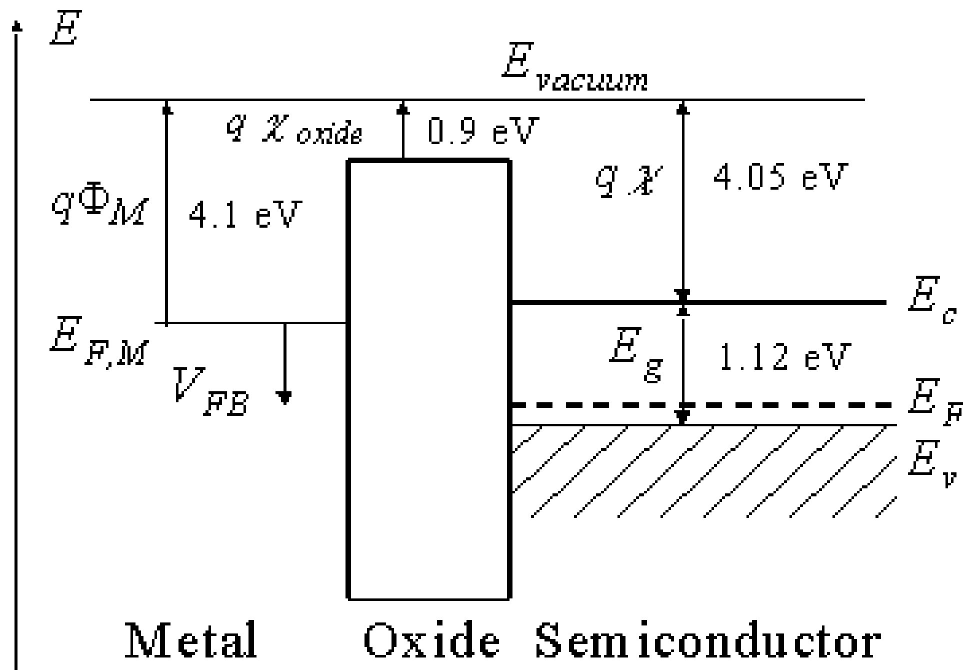
MOS Capacitors

The oxide is modeled as a semiconductor with a very large bandgap and blocks any flow of carriers between the semiconductor and the gate metal. The band bending in the semiconductor is consistent with the presence of a depletion layer. At the semiconductor-oxide interface, the Fermi energy is close to the conduction band edge as expected when a high density of electrons is present. The semiconductor remains in thermal equilibrium even when a voltage is applied to the gate.



Energy band diagram of an MOS structure biased in inversion.

MOS: Flat-band diagram



Flatband energy diagram of a metal-oxide-semiconductor (MOS) structure consisting of an aluminum metal, silicon dioxide and silicon.

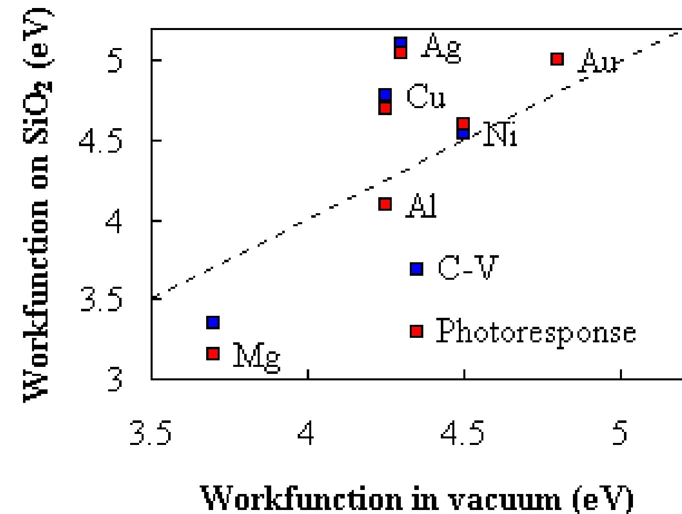
A voltage, V_{FB}, must be applied to obtain this flat band diagram. Indicated on the figure is also the work function of the aluminum gate, ϕ_M, the electron affinity of the oxide, χ_{oxide}, and that of silicon, χ, as well as the bandgap energy of silicon, E_g.

MOS Capacitors: Voltage Calculation

If there is no charge present in the oxide or at the oxide-semiconductor interface, the flatband voltage simply equals the difference between the gate metal workfunction, ϕ_M, and the semiconductor workfunction, , ϕ_S.

$$V_{FB} = \Phi_M - \Phi_S$$

	Ag	Al	Au	Cr	Mg	Ni
Φ_M (in vacuum)	4.3	4.25	4.8	4.25	3.7	4.5
Φ_M (on SiO_2) (*C-V*)	5.1	4.1	5	4.7	3.35	4.55



$$\Phi_M - \Phi_S = \Phi_M - \chi - \frac{E_g}{2q} - V_t \ln(\frac{N_a}{n_i})$$

MOS Capacitors: Voltage Calculation

Example 6.1 Calculate the flatband voltage of a silicon nMOS capacitor with a substrate doping $N_a = 10^{17}$ cm^{-3} and an aluminum gate ($\phi_M = 4.1$ V). Assume there is no fixed charge in the oxide or at the oxide-silicon interface.

$$V_{FB} = \Phi_{MS} = \Phi_M - \chi - \frac{E_g}{2q} - V_t \ln \frac{N_a}{n_i}$$

$$= 4.1 - 4.05 - 0.56 - 0.026 \times \ln \frac{10^{17}}{10^{10}} = -0.93 \text{ V}$$

Experimental Values

	Aluminum	p^+ poly	n^+ poly
nMOS	-0.93 eV	0.14 eV	-0.98 eV
pMOS	-0.09 eV	0.98 eV	-0.14 eV